REMARKS

This Amendment is in response to the Office Action mailed December 5, 2003.

The Examiner raised objections to claims 1, 2, 4-7, 23-25 and 27 because of several informalities set forth on pages 2-4 of the Office Action. In response, applicants have reviewed the Examiner's objections and except for claim 27 have amended the claims in accordance with the suggestions.

Regarding claim 27 the way the Examiner suggests could make the claim confusing and difficult to understand. However, applicants have reviewed claim 27 and it has been amended to overcome any informalities that may have been present in the claim.

Claims 1-9, 23, 24 and 26-28 are rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. The specific indefiniteness that the Examiner addresses are set forth on pages 5-7 of the office action. Applicants have reviewed the Examiner's position and each of the claims and have amended them so that any indefiniteness that may have been in the claims are now eliminated.

Regarding claim 9 the Examiner after reciting the steps in the algorithm states: "it is unclear to the Examiner how these limitations correspond to the claimed invention of parent claim 1". In response, claim 9 has been amended to state the controller which executes a program according to the process set forth in the claim to select one of the N different memories in which data is to be written. Simply stated, claim 9 sets forth an algorithm which is executed on a controller which is associated with the arbiter set forth

in claim 1 to select a memory in which data is to be written. It is believed that the claim 9 relationship to claim 1 is now clear and the rejection should now be withdrawn.

Claims 1-4, 25 and 26 are rejected under 35 USC 102(e) as being anticipated by Bass et al, US Patent 6,460,120. The argument in support of the rejection is set forth on pages 8-10. Applicants have reviewed the argument in detail and disagree with the Examiner that Bass et al. anticipates claims 1-4, 25 and 26.

Before addressing the rejection a review as it pertains to the law of anticipation will be given. Under 35 USC 102 (anticipation) every element and function set forth in a claim must be shown and/or described in a single reference. In the event a reference failed to disclose an element of a claim the way the element is interconnected and/or the function of the element then the claim is not anticipated by the reference. Applying the law to applicants' claim 1 it is applicants' contention that the reference does not teach a single arbiter responsive to a request signal and performing the function as set forth in the claim. In contrast, Bass et al. teaches multiple arbiters, each one controlling a separate chip. Failure of Bass et al. to disclose the single arbiter responding to signal and performing the functions set forth in the claim makes claim 1 and the dependent claim patentable over the Bass et al. reference.

Pertaining to claims 25 and 26 the amended claims specifically call for providing a single arbiter to grant access to the plurality of separate memories. As argued above and incorporate herein by reference that feature is not present in the reference. Therefore, the reference does not anticipate the claim. It is also noted that claim 25 calls for a simultaneous reading of memories. That process step of reading memories simultaneously is not present in Bass et al. where the memories are read singly and not

simultaneously as is required by the process. As a consequence, claims 25 and 26 are not anticipated by the reference.

Claim 23 is rejected under 35 USC 102(e) as being anticipated by Bartoldus et al. (U.S. Patent 6,560,227). In response, claim 23 is canceled without prejudice.

Claim 24 is rejected under 35 USC 103(a) as being obvious over Bartoldus et al. (U.S. Patent 6,560,227) in view of Bass et al (U.S. Patent 6,460,120). The Examiner seems to rely on Bartoldus et al. for allegedly teaching partitioning the frame whereas the Examiner relies on Bass for allegedly teaching multiple different memories. The Examiner then concludes that it would be obvious to form the combination because then the requested data could be retrieved from the memories in a quicker fashion and use less processing cycles.

In response, applicants respectfully disagree with the Examiner and argue that the reference teaches away from the claims in amended form. In particular, claim 24 calls for a single arbiter in response to a request causing the plurality of memory elements to be read simultaneously. In contrast and as argued above relative to Bass et al. a plurality of memory arbiter one for each memory element is disclosed whereas the claim calls for a single memory arbiter controlling multiple memories. It is applicants' contention that the teaching in Bass et al. is inapposite to that of the claimed invention. Therefore, an artisan viewing these two references would not form the Examiner's combination since one of the references teaches away from the claimed invention.

In addition, applicants argue that the single arbiter performing functions recited in claim 24 provide a novel process. In addition to the novel process accessing multiple memories simultaneously to generate data with sufficient bandwidth for a FAT pipe

provides a benefit to the user which is not recognized in the reference. In the reference there is no need to access multiple data since a FAT pipe is not contemplated. It is applicants' contention that novel process step together with benefits, increase in bandwidth of data, are indicia of unobviousness. As a consequence, claim 24 is not obvious in view of the references.

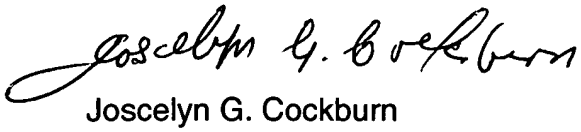
Claim 27 is rejected under 35 USC 103(a) as being obvious over Bartoldus et al. (U.S. Patent 6,560,227) in view of Bass et al. (U.S. Patent 6,460,120) and applicants' admitted prior art. The Examiner's argument in supporting this rejection is set forth on pages 13-16 of the Office Action. The Examiner's argument has been reviewed in detail but for brevity is not repeated here.

In response to the Examiner's argument applicants respectfully disagree with the Examiner and argue that the reference single or in combination does not suggest simultaneously accessing with a single arbiter multiple memory modules in a single memory access window and performing the actions recited in the claim. As argued above this portion of the process is novel and provides benefit to the user. The benefit is that a high bandwidth port can be supported from a plurality of these memories controlled by a single arbiter. It is applicants' contention that the novel process coupled with benefits are indicia of unobviousness. As a consequence, claim 27 is not obvious in view of the reference.

Newly added claims 29-34 are also patentable over the art of record for reasons including those argued above.

It is believed that the present amendment answers all the issues raised by the Examiner. Reconsideration is hereby requested and an early allowance of all the claims is solicited.

Respectfully Submitted,



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